NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE AND METHOD OF MANUFACTURING THE SAME

Japanese Patent Application No. 2003-54451, filed on February 28, 2003, is hereby incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

The present invention relates to a non-volatile semiconductor memory device including a non-volatile memory element which is controlled by a word gate and a select gate.

As an example of a non-volatile semiconductor memory device, a MONOS (Metal-Oxide-Nitride-Oxide-Semiconductor or -Substrate) non-volatile semiconductor memory device is known. In the MONOS non-volatile semiconductor memory device, a gate insulating film between a channel and a gate is formed of a laminate consisting of a silicon oxide film, a silicon nitride film, and a silicon oxide film, and a charge is trapped in the silicon nitride film.

As such a MONOS non-volatile semiconductor memory device, a MONOS flash memory cell including a non-volatile memory element (MONOS memory element) controlled by one select gate and one control gate is disclosed (see Japanese Patent Application Laid-open No. 6-181319, Japanese Patent Application Laid-open No. 11-74389, U.S. Patent No. 5,408,115, and U.S. Patent No. 5,969,383, for example).

BRIEF SUMMARY OF THE INVENTION

The present invention may provide a non-volatile semiconductor memory device having a small layout area.

According to a first aspect of the present invention, there is provided a non-volatile semiconductor memory device comprising: